IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
SWAMI

Serial No. **NOT YET ASSIGNED**

Filing Date: **HEREWITH**

For: **AN IMPROVED LOOK-UP TABLE APPARATUS TO PERFORM TWO-BIT ARITHMETIC OPERATION INCLUDING CARRY GENERATION**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL 768137995 US
DATE OF DEPOSIT: February 14, 2002
NAME: Dawn Kimler
SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 1 as prior art. Also, certain labels and signal connections are being corrected in FIGS. 4 and 5 for consistency with the specification. No new matter is being added.

In the Claims:

Please cancel Claims 1 to 11.

Please add new Claims 12 to 39.

12. A programmable look-up table apparatus comprising:

a plurality of programmable data storage cells each providing a cell output signal indicative of data stored therein;

means for selecting one of said cell output signals as an output signal and comprising

a plurality of successive selection means each being responsive to a respective one of a plurality of input signals,

a first selection means selecting one of two mutually exclusive and collectively exhaustive subsets of the cell output signals, and each successive selection means selecting one of two mutually exclusive and collectively exhaustive subsets of cell output signals selected by a preceding selection means until a last selection means produces the output signal;

the look-up table apparatus being divided into equal first and second halves, excluding said last selection means, where each half comprises half of the remaining selection means, half of said programmable data storage cells, and half of the input signals;

first means for selecting a selection input for a final selection means in each of said first and second halves to be a first input signal from the second half during a normal mode and a carry out signal from a previous bit operation during a two-bit arithmetic mode, said last

selection means receiving a second input signal from the second half; and

second means for connecting an output from said final selection means of said first half as a least significant output bit of the two-bit arithmetic operation and for connecting an output of said final stage of said second half as a most significant output bit of the two-bit arithmetic operation during the arithmetic mode, said second means also allowing normal selection operation using one of the input signals during the normal mode.

13. The programmable look-up table apparatus of Claim 12 further comprising means for selectively applying at least one input signal of said second half and said first half as the first input signal to said second half.

14. The programmable look-up table apparatus of Claim 12 further comprising additional logic means connected to each half for generating the carry out signal for the corresponding bit operation and a sum output.

15. The programmable look-up table apparatus of Claim 14 wherein said additional logic means comprises an exclusive OR gate receiving the output from the final selection means of a respective half as a selection signal for selecting at least one of a carry in signal and the second input signal to generate the carry out signal.

16. The programmable look-up table apparatus of Claim 12 wherein the look-up table apparatus further has a counting mode of operation; and further comprising a respective storage element connected to the output of each half for storing the result of a previous arithmetic operation for use as an input to each respective half for performing counting during the counting mode.

17. The programmable look-up table apparatus of Claim 12 wherein said first means in each half comprises a multiplexer.

18. The programmable look-up table apparatus of Claim 12 wherein said second means comprises a logic gate.

19. The programmable look-up table apparatus of Claim 12 wherein said logic gate comprises an AND gate.

20. The programmable look-up table apparatus of Claim 12 wherein said first means for each half receives the first input signal from the other half during the normal mode and the carry out signal from the least significant bit operation during the arithmetic mode; and wherein said last selection means comprises a logic gate receiving as inputs a last selection signal from each half to enable the look-up table to function as at least one of a single look-up table of n inputs or two independent look-up tables of n-1 inputs, each in the normal mode, while retaining the functionality of the arithmetic mode of operation.

21. A programmable look-up table apparatus comprising:

a plurality of programmable data storage cells each providing a cell output signal indicative of data stored therein;

a plurality of successive selection stages each being responsive to a respective one of a plurality of input signals, a first selection stage selecting one of two mutually exclusive subsets of the cell output signals, and each successive selection stage selecting one of two mutually exclusive subsets of cell output signals selected by a preceding selection stage until a last selection stage produces an output signal;

the look-up table apparatus being divided into equal first and second halves, excluding said last selection stage, where each half comprises half of the remaining selection stages, half of said programmable data storage cells, and half of the input signals;

first circuitry for selecting a selection input for a final selection stage in each of said first and second halves to be a first input signal from the second half during a normal mode and a carry out signal from a previous bit operation during a two-bit arithmetic mode, said last selection stage receiving a second input signal from the second half; and

second circuitry for connecting an output from said final selection stage of said first half as a least significant output bit of the two-bit arithmetic operation and

for connecting an output of said final stage of said second half as a most significant output bit of the two-bit arithmetic operation during the arithmetic mode.

22. The programmable look-up table apparatus of Claim 21 wherein said second circuitry also allows normal selection operation using one of the input signals during the normal mode.

23. The programmable look-up table apparatus of Claim 21 further comprising a circuit for selectively applying at least one input signal of said second half and said first half as the first input signal to said second half.

24. The programmable look-up table apparatus of Claim 21 further comprising at least one logic device connected to each half for generating the carry out signal for the corresponding bit operation and a sum output.

25. The programmable look-up table apparatus of Claim 24 wherein said at least one logic device comprises an exclusive OR gate receiving the output from the final selection stage of a respective half as a selection signal for selecting at least one of a carry in signal and the second input signal to generate the carry out signal.

26. The programmable look-up table apparatus of Claim 21 wherein the look-up table apparatus further has a counting mode of operation; and further comprising a

respective storage element connected to the output of each half for storing the result of a previous arithmetic operation for use as an input to each respective half for performing counting during the counting mode.

27. The programmable look-up table apparatus of Claim 21 wherein said first circuitry in each half comprises a multiplexer.

28. The programmable look-up table apparatus of Claim 21 wherein said second circuitry comprises a logic gate.

29. The programmable look-up table apparatus of Claim 21 wherein said logic gate comprises an AND gate.

30. A programmable logic device comprising:

a plurality of programmable look-up table apparatuses each comprising

a plurality of programmable data storage cells each providing a cell output signal indicative of data stored therein,

a plurality of successive selection stages each being responsive to a respective one of a plurality of input signals, a first selection stage selecting one of two mutually exclusive subsets of the cell output signals, and each successive selection stage selecting one of two mutually exclusive subsets of cell output signals selected by a preceding

selection stage until a last selection stage produces an output signal,

each look-up table apparatus being divided into equal first and second halves, excluding said last selection stage, where each half comprises half of the remaining selection stages, half of said programmable data storage cells, and half of the input signals,

first circuitry for selecting a selection input for a final selection stage in each of said first and second halves to be a first input signal from the second half during a normal mode and a carry out signal from a previous bit operation during a two-bit arithmetic mode, said last selection stage receiving a second input signal from the second half, and

second circuitry for connecting an output from said final selection stage of said first half as a least significant output bit of the two-bit arithmetic operation and for connecting an output of said final stage of said second half as a most significant output bit of the two-bit arithmetic operation during the arithmetic mode.

31. The programmable logic device of Claim 30 wherein said second circuitry of each programmable look-up table apparatus also allows normal selection operation using one of the input signals during the normal mode.

32. The programmable logic device of Claim 30 wherein each programmable look-up table apparatus further comprises a circuit for selectively applying at least one input signal of said second half and said first half as the first input signal to said second half.

33. The programmable logic device of Claim 30 wherein each programmable look-up table apparatus further comprises at least one logic device connected to each half for generating the carry out signal for the corresponding bit operation and a sum output.

34. The programmable logic device of Claim 33 wherein said at least one logic device comprises an exclusive OR gate receiving the output from the final selection stage of a respective half as a selection signal for selecting at least one of a carry in signal and the second input signal to generate the carry out signal.

35. The programmable logic device of Claim 30 wherein the look-up table apparatus further has a counting mode of operation; and further comprising a respective storage element connected to the output of each half for storing the result of a previous arithmetic operation for use as an input to each respective half for performing counting during the counting mode.

36. A method for configuring a programmable look-up table apparatus comprising a plurality of programmable data

storage cells each providing a cell output signal indicative of data stored therein, a plurality of successive selection stages each being responsive to a respective one of a plurality of input signals, a first selection stage selecting one of two mutually exclusive subsets of the cell output signals, and each successive selection stage selecting one of two mutually exclusive subsets of cell output signals selected by a preceding selection stage until a last selection stage produces an output signal, the method comprising:

dividing the look-up table apparatus into equal first and second halves, excluding the last selection stage, where each half comprises half of the remaining selection stages, half of the programmable data storage cells, and half of the input signals;

selecting a selection input for a final selection stage in each of the first and second halves to be a first input signal from the second half during a normal mode and a carry out signal from a previous bit operation during a two-bit arithmetic mode, the last selection stage receiving a second input signal from the second half; and

connecting an output from the final selection stage of the first half as a least significant output bit of the two-bit arithmetic operation and connecting an output of the final stage of the second half as a most significant output bit of the two-bit arithmetic operation during the arithmetic mode.

37. The method of Claim 36 further comprising selectively applying at least one input signal of the second

half and the first half as the first input signal to the second half.

38. The method of Claim 36 further comprising generating the carry out signal for the corresponding bit operation and a sum output using at least one logic device.

39. The method of Claim 36 wherein the look-up table apparatus further has a counting mode of operation; and further comprising storing the result of a previous arithmetic operation in a respective storage element connected to the output of each half for use as an input to each respective half for performing counting during the counting mode.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner=s convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability.

Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

In re Patent Application of:
SWAMI
Serial No. **Not Yet Assigned**
Filed: **Herewith**

Respectfully submitted,

JOHN F. WOODSON, II
Reg. No. 45,236
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicants

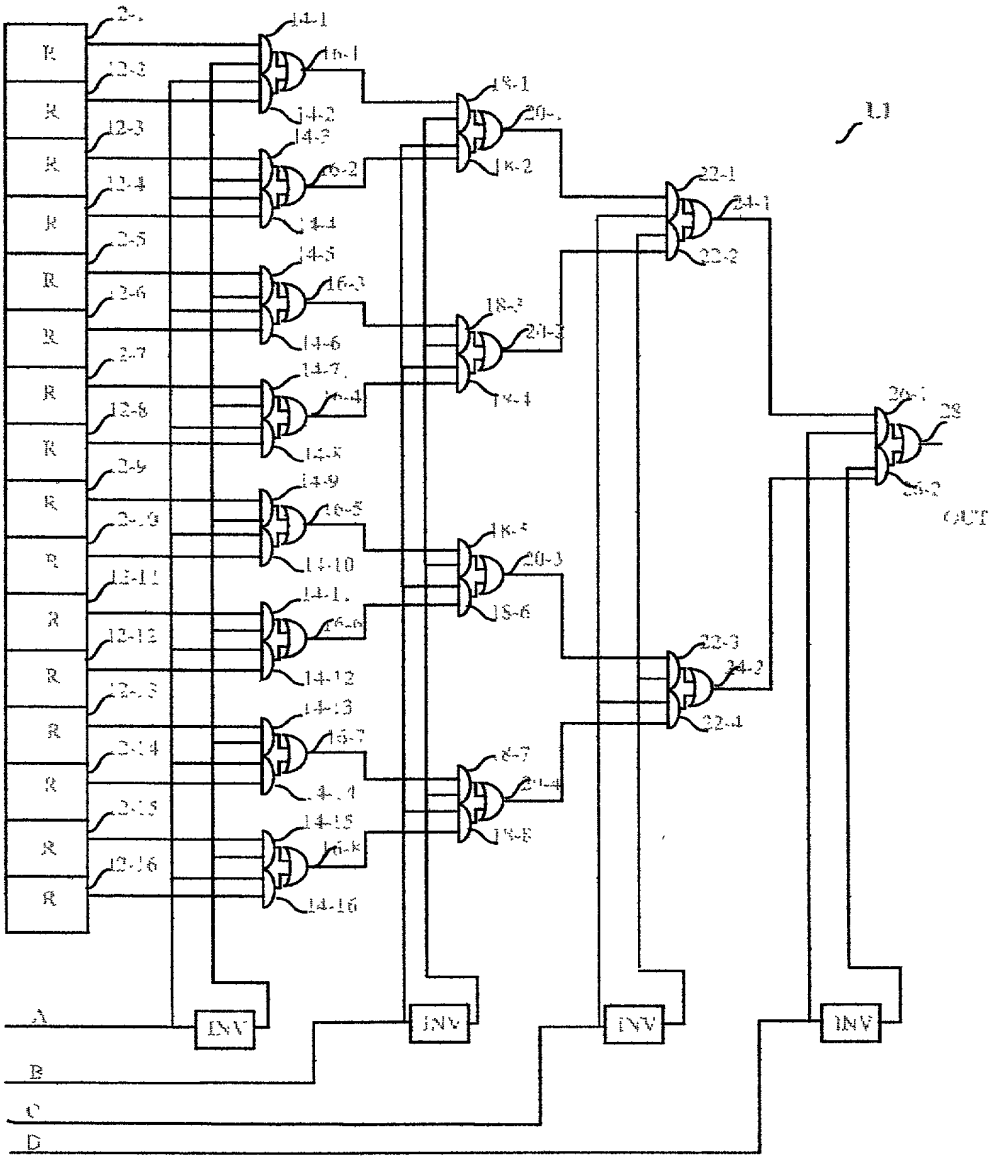

FIG1

(PRIOR ART)

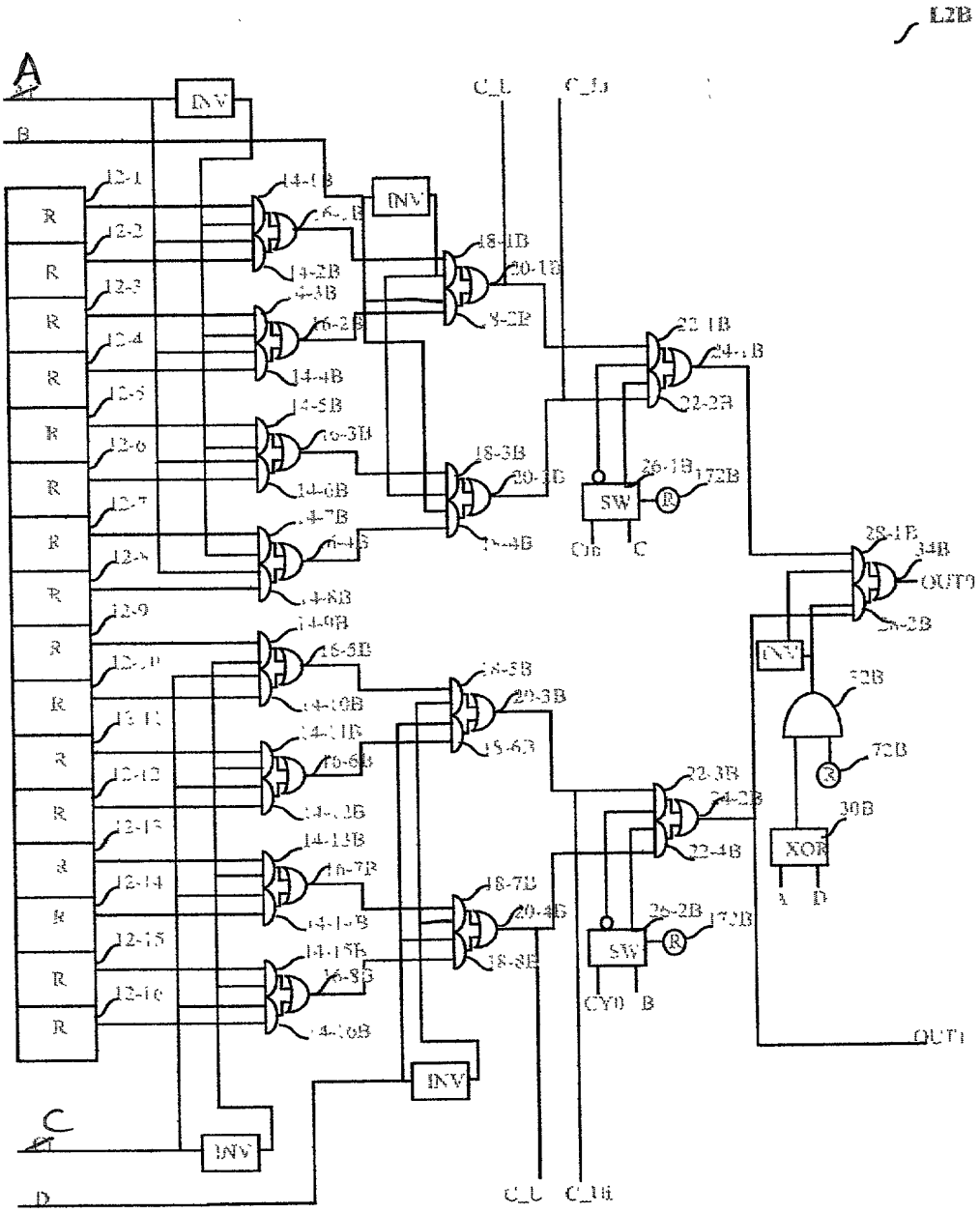

FIG4

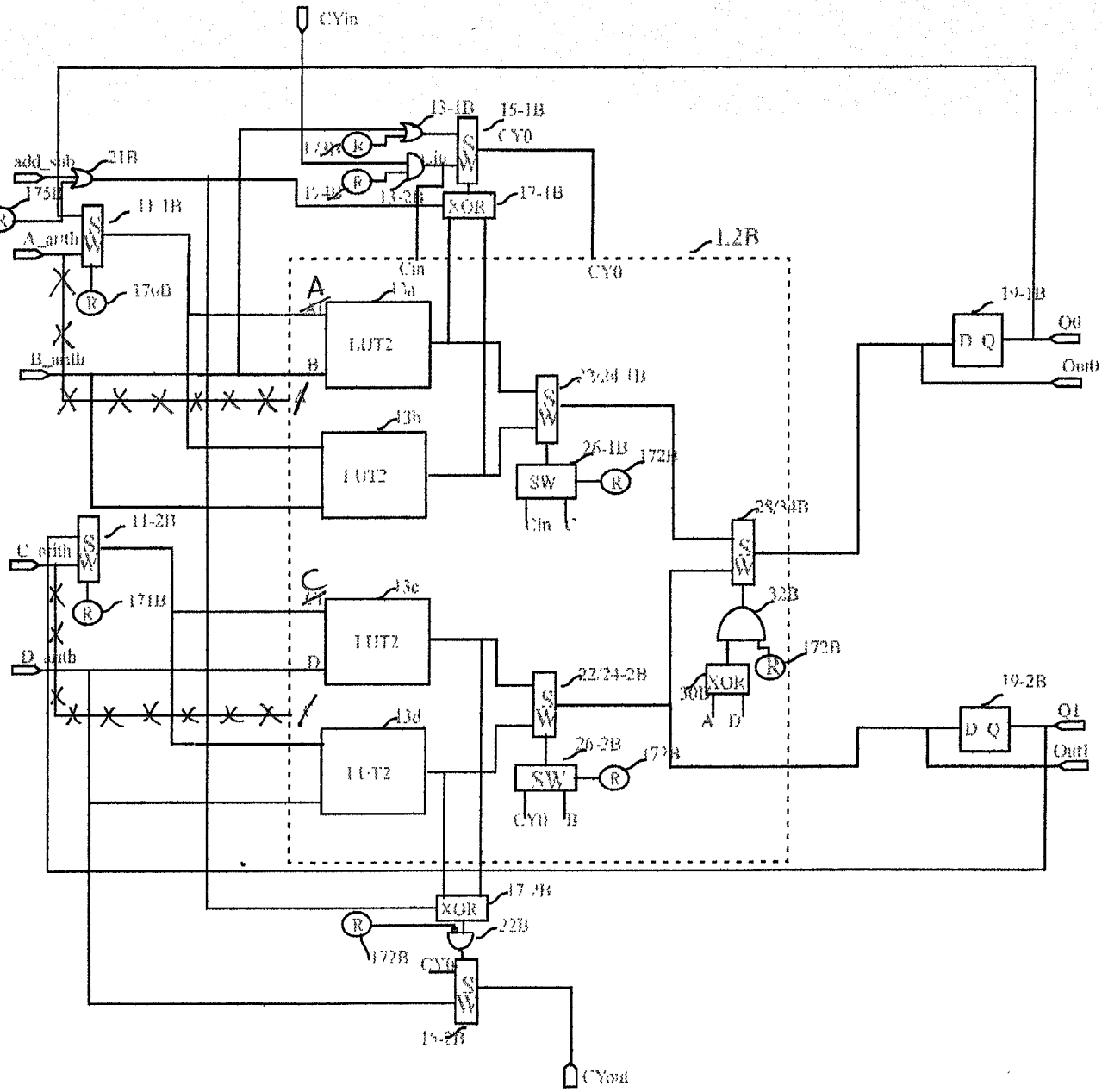
CYin
15-1B
15-1B
CY0
add_sub
21B
17-1B
XOR
L2B
Cin
CY0
A
LUT2
19-1B
Q0
Out0
B_addb
B
23/24-1B
26-1B
172B
SW
Cin
11-2B
C_addb
17IB
C
LUT2
32B
172B
XOR
30B
A
D
22/24-2B
19-2B
Q1
Out1
D_addb
D
26-2B
CY0
B
17-2B
XOR
172B
22B
CYout

FIG5